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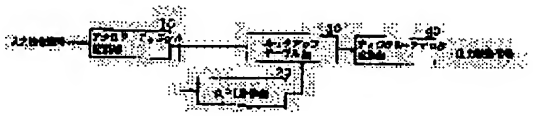
(54) METHOD FOR IMPROVING SCENE ADAPTIVE VIDEO AND CIRCUIT THEREFOR

(57)Abstract:
PURPOSE: To obtain a video signal whose contrast is improved through adaptively correcting brightness by making different input and output characteristics according to the value of the average brightness level of an input video signal.
CONSTITUTION: An analog/digital converting part 10 converts a video signal inputted in an analog signal configuration into a digital signal. An APL calculating part 20 and a lookup table part 30 are connected with the output edge of the analog/digital converting part 10. The APL calculating part 20 inputs a video signal outputted from the analog/digital converting part 10, and calculates an nAPL value. The lookup table part 30 corrects the output signal of the analog/digital converting part 10 by the APL value outputted from the APL calculating part 20, and outputs it. The output signal of the lookup table part 30 is impressed to a digital/analog converting part 40, and converted into an analog video signal.



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(54)【発明の名称】　場面適応映像改善方法及びその回路

(57)【特許請求の範囲】

【請求項１】　平均明るさレベルを用いて映像信号の明るさと対比を調節する方法において、

入力映像信号が有し得る平均明るさレベルの範囲を多数の領域に分割する段階と、

前記領域のそれぞれに相異なる入出力特性を設定する段階と、

入力映像信号に対する所定期間の平均明るさレベルを計算する段階と、

前記計算された平均明るさレベルに対応する入出力特性により入力映像信号を調節して出力する段階を含む場面適応映像改善方法。

【請求項２】　前記領域分割段階は映像信号の対比を改善する効果が大となるよう多数の領域に分割することを特徴とする請求項１記載の場面適応映像改善方法。

【請求項３】　前記領域は暗い場面に対応する平均明るさレベルの第１領域、中間程度の平均明るさレベルの第２領域、前記第１領域と第２領域との間の平均明るさレベルを有する第３領域、及び前記第２領域より高い平均明るさレベルを有する第４領域からなり、

入力映像信号が有し得る平均明るさレベルの範囲をそれに対応する０と１との間の範囲に変換する場合、第１領域は０近くの平均明るさレベルを有し、第２領域は０・５を含み０・５近くの平均明るさレベルを有することを特徴とする請求項２記載の場面適応映像改善方法。

【請求項４】　前記調節段階は計算された平均明るさレベルが第１領域に属する場合、入力映像信号をそのまま出力することを特徴とする請求項３記載の場面適応映像改善方法。

【請求項５】　前記調節段階は計算された平均明るさレ

ベルが第２領域に属する場合、対比向上のための次の式、

OUT＝ｙ３（ｘ）

ｙ３（ｘ）＝xL^2，

ｙ３（ｘ）＝$xH^{0.5}$

ここで、ＯＵＴは補正された映像信号、ｘＬは０～０．５期間、ｘＨは０．５～１期間である、

＊

OUT＝ａｍｐ×ａｂｓ［ｍ－ａｂｓ（ｎＡＰＬ－ｍ）］×ｙ３（ｘ）

ｙ３（ｘ）＝xL^2，ｙ３（ｘ）＝$xH^{0.5}$

ここで、ＯＵＴは補正された映像信号、ａｍｐは増幅度、ａｂｓは絶対値、ｎＡＰＬは正規化された平均画像レベル値であり、通常的にｍは０．５であり、ｘＬは０～０．５期間、ｘＨは０．５～１期間である、

により映像信号のレベルｘを補正した映像信号を出力す※

OUT＝ａｍｐ１×ａｂｓ（ｍ－ａｂｓ（ｍ－ｎＡＰＬ（１））×ｙ３１（ｘ）＋ａｍｐ２×ａｂｓ（ｍ－ａｂｓ（ｎＡＰＬ（ｈ）－ｍ））×ｙ３ｈ（ｘ）

ｙ３１（ｘ）＝xL^2，ｙ３ｈ（ｘ）＝$xH^{0.5}$

ここで、ＯＵＴは補正された映像信号で、ｍは通常的に０．５であり、ａｍｐ１，ａｍｐ２はｍ以下と以上の増幅度、ａｂｓは絶対値、ｎＡＰＬ（ｌ）とｎＡＰＬ（ｈ）はそれぞれｍ以下と以上の入力信号に対して計算した正規化されたＡＰＬ値、ｘＬは０～０．５期間、ｘＨは０．５～１期間である、により映像信号のレベルｘを補正した映像信号を出力することを特徴とする請求項３記載の場面適応映像改善方法。

【請求項８】　前記調節段階は計算された平均明るさレベルが第３領域に属する場合、対比向上のための次の式、

OUT=abs(abs(p-q)/p) ×y1(x)，

$y1(x)=x^{0.5}$，

p=a__area-period/2, q=abs(a__area__center-nAPL)

ここで、ＯＵＴは補正された映像信号、ａｂｓは絶対値、a__area-period はａ領域の期間を示し、a__area__centerはａ領域の中心値、ｎＡＰＬは正規化された平均画像レベル値である、

により映像信号のレベルｘを補正した映像信号を出力することを特徴とする請求項３記載の場面適応映像改善方法。

【請求項９】　前記調節段階は計算された平均明るさレベルが第１領域または第１領域に属する場合、対比向上のための次の式、

OUT=(0.5-nAPL)×y1(x)，

$y1(x)=x^{0.5}$，

ここで、ＯＵＴは補正された映像信号、ｎＡＰＬは正規化された平均画像レベル値である、

により映像信号のレベルｘを補正した映像信号を出力することを特徴とする請求項３記載の場面適応映像改善方法。

【請求項１０】　前記調節段階は計算された平均明るさ

＊により入力映像信号のレベルｘを補正した映像信号を出力することを特徴とする請求項３記載の場面適応映像改善方法。

【請求項６】　前記調節段階は計算された平均明るさレベルが第２領域に属する場合、対比向上のための次の式、

＊

OUT＝ａｍｐ×ａｂｓ［ｍ－ａｂｓ（ｎＡＰＬ－ｍ）］×ｙ３（ｘ）

※ることを特徴とする請求項３記載の場面適応映像改善方法。

【請求項７】　前記調節段階は計算された平均明るさレベルが第２領域に属する場合、対比向上のための次の式、

OUT＝ａｍｐ１×ａｂｓ（ｍ－ａｂｓ（ｍ－ｎＡＰＬ（１））×ｙ３１（ｘ）＋ａｍｐ２×ａｂｓ（ｍ－ａｂｓ（ｎＡＰＬ（ｈ）－ｍ））×ｙ３ｈ（ｘ）

レベルが第４領域に属する場合、対比向上のための次の式、

OUT=amp ×abs(nAPL-m) ×y2(x), y2(x)=pow(x,2)

ここで、ＯＵＴは補正された映像信号であり、ｍは通常的に０・５であり、ａｍｐは増幅度、ａｂｓは絶対値、ｎＡＰＬは正規化されたＡＰＬ値である、

により映像信号のレベルｘを補正した映像信号を出力することを特徴とする請求項３記載の場面適応映像改善方法。

【請求項１１】　平均明るさレベルを用いて映像信号の明るさと対比を調節して出力する装置において、

入力端を通じて入力される映像信号の所定期間の平均明るさレベルを計算する手段、

入力映像信号が有し得る平均明るさレベルの範囲を多数の領域に分割され、入力映像信号を各領域で相異なる多数の入出力特性を備え、前記計算された平均明るさレベルに対応する入出力特性により入力映像信号を調節して出力する手段を含む場面適応映像改善回路。

【請求項１２】　前記調節手段は前記平均明るさレベルに対応するそれぞれの明るさ訂正特性を入力映像信号に対応する出力映像信号から構成されたルックアップテーブルの形態に貯蔵することを特徴とする請求項１１記載の場面適応映像改善回路。

【請求項１３】　前記調節手段は平均明るさレベルの計算に用いられた入力映像信号に続いて入力する映像信号の明るさ及び対比を訂正することを特徴とする請求項１１記載の場面適応映像改善回路。

【請求項１４】　前記調節手段の前段に位置し、平均明るさレベルの計算に用いられた入力映像信号の明るさ及び対比を調節しうるよう入力端を通じて印加される入力映像信号を遅延して出力する遅延器をさらに備えることを特徴とする請求項１１記載の場面適応映像改善回路。

【請求項１５】　前記入力端を通じて印加される映像信

号を平均明るさレベル計算手段により計算された平均明るさレベルにより可変される増幅率に増幅して前記調節手段に出力する増幅部をさらに備えることを特徴とする請求項１１記載の場面適応映像改善回路。

【請求項１６】　前記増幅部は計算された平均明るさレベルの値が１に近い値の場合は、入出力特性曲線の勾配が小さくなるよう入力された映像信号を増幅し、平均明るさレベルの値が０に近い値の場合は入出力特性曲線の勾配が大きくなるよう映像信号を増幅して出力させることを特徴とする請求項１１記載の場面適応映像改善回路。

【請求項１７】　前記平均明るさレベル計算手段は入力映像信号の低域成分のみを通過させ平均明るさレベルの値を計算してそれに対応する電圧を出力する低域通過フィルタと、

前記低域通過フィルタから印加された電圧により明るさ及び対比調節手段を制御するための信号を出力するディコーダから構成されることを特徴とする請求項１１記載の場面適応映像改善回路。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は映像信号の明るさ及び対比を調節するための方法及び回路に係り、さらに詳しくは場面の平均明るさレベルにより映像信号の明るさ及び対比を適応的に調節できる場面適応映像改善方法及びその回路に関する。

【０００２】

【従来の技術】自然照明は極めて広い明るさ領域と対比領域を有しており、人間の視覚特性もこれに対応できるほどに適応的に動作するので、人間は陰の隅々までも容易に認識できる。しかし、カメラやＴＶなどは自然照明＊

＊に適合でない。カラーカメラは特定の照明領域を有する入力光に応答できるが、カメラの電気的な出力信号が例えば１ボルトピーク－対－ピーク（ｐｅａｋ－ｔｏ－ｐｅａｋ）の信号に限られるので、通常の顕示機器は対比領域が極めて狭くなって劣化された画像を顕示する場合は頻繁に発生している。

【０００３】アメリカ特許第４，１５２，７２０号の対比訂正装置とアメリカ特許第４，４８９，３４９号の画像明るさ調節回路は明るさ調節により対比を調節する方式であって、このような問題点の解決を図った。アメリカ特許第４，１５２，７２０号の対比訂正装置はカメラに対するユーザーの外部調節値により映像信号の入出力特性を相違に調節することにより部分的に相対的な対比向上をなした。図１は従来の対比訂正装置で使われた入出力特性を示したグラフであって、ｙ１（ｘ）＝$x^{0.5}$とｙ２（ｘ）＝x^{2}と表示された二つの特性曲線（ｙ１，ｙ２）を示す。しかし、図１と関連した先行技術は明るさ調節に基づき対比を改善させ、対比改善は事実上明るさ調節の付加的な効果として部分的にのみなされ、特に手動操作の問題点があった。

【０００４】アメリカ特許第４，４８９，３４９号の画像明るさ調節回路は前者の場合に比べて一歩発展した形態で、入力映像信号の平均画像レベル（以下、ＡＰＬと称する）により入出力特性を前者の場合と類似に調節するもので、前者の場合に比べてＡＰＬにより適応的に動作させたことは前者の場合と異なるが、その効果は前者の場合と類似である。

【０００５】図２はアメリカ特許第４，４８９，３４９号による入出力特性を示す。図２の入出力特性を式で表現すれば次の通りである。

$$OUT = nAPL \times y2(x) + (1 - nAPL) \times y1(x)$$

ここで、ｎＡＰＬは正規化された平均画像レベルであって、入力映像信号の平均画像レベルであり、ｙ１（ｘ），ｙ２（ｘ）は図１に示したものと同一な入出力特性曲線である。上記式によれば、出力ＯＵＴはｎＡＰＬと１－ｎＡＰＬに対してｙ１（ｘ）とｙ２（ｘ）が加重された形態となる。例えば、ｎＡＰＬが０．３の時ＯＵＴ＝０．３×ｙ２（ｘ）＋０．７×ｙ１（ｘ）となり、ｎＡＰＬが０．７ならＯＵＴ＝０．７×ｙ２（ｘ）＋０．３×ｙ１（ｘ）となる。従って、ｎＡＰＬが０．３のように低い値を有した時はｙ１にさらに大きい加重値を置いて全体的な平均画像レベルの値を上げ、ｎＡＰＬが０・７の時はその反対の場合にｙ２にさらに大きい加重値を置いて全体的な平均画像レベルの値が下げられる。

【０００６】図２において、ｎＡＰＬが０．５より低い場合は＋方向に、ｎＡＰＬが０．５より大きい場合は－方向に変化量が原信号に加えられる。従って、ｎＡＰＬが両端の０または１に近くなるほど入力映像信号の平均画像レベルが大きく変わり、ｎＡＰＬが０．５辺りの値の場合はその平均画像レベルが小さく変わる。この技術もやはり画像の明るさに関連した平均画像レベルを用いて対比を調節するが、明るさ処理に重点を置くことにより対比効果が劣る。従って、夜の風景のように極めて暗い画面は明るさを上げる結果によりかえって不自然な画面を出力することになる問題点があった。

【０００７】

【発明が解決しようとする課題】本発明の目的は入力映像信号の平均画像レベルが有し得る範囲を多数の領域に区分し、各領域毎に相異なる入出力特性を与え、入力映像信号の平均画像レベルに対応する領域の入出力特性により入力映像信号の明るさを調節することにより、従来の技術に比べて改善された対比の画像が得られる場面適応映像改善方法を提供することである。

【０００８】本発明の他の目的は前述した方法を具現した場面適応映像改善回路を提供することである。

【０００９】

【課題を解決するための手段】前述した目的を達成するために、本発明は平均明るさレベルを用いて映像信号の明るさと対比を調節する方法において、入力映像信号が有し得る平均明るさレベルの範囲を多数の領域に分割する段階と、前記領域のそれぞれに相異なる入出力特性を設定する段階と、入力映像信号に対する所定期間の平均明るさレベルを計算する段階と、前記計算された平均明るさレベルに対応する入出力特性により入力映像信号を調節して出力する段階を含む。

【００１０】本発明の他の目的を達成するために、平均明るさレベルを用いて映像信号の明るさと対比を調節して出力する装置において、入力端を通じて入力される映像信号の所定期間の平均明るさレベルを計算する手段、入力映像信号が有し得る平均明るさレベルの範囲を多数の領域に分割され、入力映像信号を各領域で相異なる多数の入出力特性を備え、前記計算された平均明るさレベルに対応する入出力特性により入力映像信号を調節して出力する手段を含む。

【００１１】

【実施例】以下、添付した図面に基づき本発明を具現した実施例を詳細に説明する。図３は本発明で使用した入出力特性を示したグラフを示す。図３において二つの曲線ｙ１及びｙ２は図１の入出力特性曲線と同一なものであり、Ｓ形態の曲線ｙ３は平均画像レベルを用いて明るさ及び対比を調節するために本発明により追加された入出力特性曲線である。特性曲線ｙ１は入力信号の全体的な明るさ上昇の低いレベル値の相対的な対比向上効果をもたらし、特性曲線ｙ２は全体的な明るさ低下と高いレベル値の相対的な対比向上効果を、そして特性曲線ｙ３は全体的な対比向上効果を奏でる。

【００１２】図４は本発明の場面適応映像改善方法における明るさ及び対比訂正特性を示したグラフを示す。図４の特性曲線は図３の入出力特性曲線ｙ１，ｙ２，ｙ３を用いた対比調節がｎＡＰＬ上で区分された領域に相異なるようなされることを示す。本発明では入力映像信号が有し得る平均画像レベルの範囲を四つの領域に区分し、各領域毎に個別の明るさ訂正特性を与える。明るさ訂正特性は入力映像信号とｎＡＰＬと図３の入出力特性曲線及び各領域毎に相異なるよう与えられる加重値により決定される。入力映像信号はかかる明るさ訂正特性により明るさ及び対比が調節される。その結果により改善された対比の映像信号が得られる。本発明の実施例で使われた入出力特性曲線を式で示せば次の通りである。

【００１３】

$y1(x) = x^{0.5}$,　$y2(x) = x^2$

$y3L(x) = xL^2$,　$y3H(x) = xH^{0.5}$

ここで、ｘＬは０～０．５の範囲を有し、ｘＨは０．５＊１～１の範囲を有する。前述した数式で指数部を０．５や２に制限する必要はなく、必要に応じて他の値に代替しても良い。

【００１４】本発明で区分される領域は図４に示した通りの四つの領域である。かかる領域の境界は明るさ及び対比訂正により適切に選択される。図４において領域表示がなされていないａ領域より低いｎＡＰＬを有する領域が残り一つの領域である。各領域の対比改善のために使われた図３の入出力特性曲線について説明すれば次の通りである。

【００１５】ｎＡＰＬ値がａ領域内に存すれば特性曲線ｙ１，ｎＡＰＬ値がｂ領域内に存すればｙ３曲線、ｎＡＰＬ値がｃ領域内に存すればｙ２曲線が明るさと対比の訂正に使われる。図３の入出力特性曲線を用いて図４のように各領域に対する対比調節をするために使われた数式についてさらに詳しく説明する。

【００１６】ａ領域より低いｎＡＰＬを有する領域は極めて暗い夜の風景などにより得られるｎＡＰＬの値を有する。この領域の場合、入力信号のレベルと出力信号のレベルを同一にさせる。こうすることにより、入力信号の明るさと出力信号の明るさが同一になって不自然な画像が得られることが防がれる。ａ領域の場合、出力信号ＯＵＴは次の式（１）により得られる。

【００１７】

$$OUT = |(p-q)/p| \times y1(x) \quad \cdots (1)$$

ここで、ｐ＝（ａ領域の区間）／２，ｑ＝｜ａ領域の中心値－ｎＡＰＬ｜と定義される。ａ領域の中心値は図４において文字ｄと示された。上記式（１）は特性曲線ｙ１に対する加重値がａ領域の区間と半分と、ａ領域の中心値とｎＡＰＬ値との差に対する絶対値により決定されることを示す。従って、出力信号ＯＵＴはｎＡＰＬ値がａ領域の中心に存する時ＯＵＴ＝ｙ１（ｘ）となり、ｎＡＰＬ値がａ領域の中心から遠くなればｃ＝｜ｐ－ｑ｜／ｐ＜１である正規化された形態のｃによりＯＵＴ＝ｃ×ｙ１（ｘ）となる。上記式（１）による特性曲線は実際に図４のようにｂ領域の中でも示される。式（１）の特性はｂ領域で使われたＳ領域と共にａ領域の特性とｂ領域の特性をスムーズに連結させる。そして、式（１）による全般的な入出力特性は左から右へ行くほどその変化量が増加し、ａ領域の中心値ｄで入出力特性の変化量が最大となる。ｂ領域において入力信号のｎＡＰＬは０．５に近い値なので、特性曲線Ｓは主に対比向上に寄与する。従って、ｎＡＰＬが０．５を基準としてその以下とその以上に対する出力信号ＯＵＴは単なる次の式（２）または（３）により求める。

【００１８】

$$OUT = y3(x) \quad \cdots (2)$$

$$OUT = amp \times |m - |nAPL - m|| \times y3(x) \quad \cdots (3)$$

ここで、通常的にｍ＝０．５であり、ａｍｐは増幅度である。さらに改善された形態としては次の式（４）のよ

うにｎＡＰＬ値により適応的に求める。

$$OUT=amp\times|m-|m-nAPL(l)||\times y3(x)+amp2\times|m-|nAPL(h)-m||\times y3h(x)\quad\cdots(4)$$

ここで、ｎＡＰＬ（ｌ）とｎＡＰＬ（ｈ）はそれぞれｍ以下と以上のレベルを有する入力映像信号を区分してｎＡＰＬ値を求めたことであり、ｙ３ｌとｙ３ｈはｙ３特性をｍを起点に分けて示した特性である。ｃ領域の場合＊

$$OUT=amp\times|nAPL-m|\times y2(x)\quad\cdots(5)$$

このように計算されたｎＡＰＬ値により該当領域の数式により入力信号が訂正される。図４において、ｃ領域の特性曲線がｂ領域内にも存するのはｂ領域とｃ領域間の特性変化量をスムーズにするためである。一方、前述し＊はｎＡＰＬ－ｍの値により特性曲線ｙ２に加重値を与える次の式（５）により求める。

【００１９】

※た領域とその下の領域における明るさ訂正特性は次の式（６）により計算することができる。

【００２０】

$$OUT=(0.5-nAPL)\times y1(x)\quad\cdots(6)$$

図５は本発明の場面適応映像改善回路の第１実施例を示したブロック構成図である。示した通り、アナログーディジタル変換部１０はアナログ信号形態に入力される映像信号をディジタル信号に変換する。アナログーディジタル変換部１０の出力端にはＡＰＬ計算部２０とルックアップテーブル部３０がそれぞれ連結される。ＡＰＬ計算部２０はアナログーディジタル変換部１０から出力された映像信号を入力されｎＡＰＬ値を計算する。ルックアップテーブル部３０はＡＰＬ計算部２０から出力されたｎＡＰＬ値によりアナログーディジタル変換部１０の出力信号を訂正して出力する。ルックアップテーブル部３０の出力信号はディジタルーアナログ変換部４０に印加されアナログ映像信号に変換される。

【００２１】図５は映像改善回路に入力された映像信号はアナログーディジタル変換部１０によりディジタル信号に変換された後、ＡＰＬ計算部２０とルックアップテーブル部３０にそれぞれ印加される。ＡＰＬ計算部２０は１フレーム期間または多数のフレーム期間の間の実際映像信号区間に対する入力映像信号のｎＡＰＬ値を計算する。この際、ｎＡＰＬの値は連続する入力フレーム毎に更新し続ける。ルックアップテーブル部３０は入力映像信号をアドレスとするルックアップテーブルの形態に四つの領域に関連して前述した明るさ訂正特性を貯蔵し、入力映像信号のレベルとそれに対応するｎＡＰＬ値により入力映像信号の明るさを訂正して出力する。従って、ＡＰＬ計算部２０からｎＡＰＬ値が入力されれば、ルックアップテーブル部３０はこの値がどの領域に属するかを判断して入力されたディジタル映像信号を該当領域の明るさ訂正特性により補正して出力する。該当技術分野の通常の技術者はかかるルックアップテーブル部３０を領域の個数と同一な四つのルックアップテーブルから構成したり、各領域に当たる数式に基づき作成するなどの多様な方法で構成し得る。ルックアップテーブル部３０から読み出されたディジタル信号はディジタルーアナログ変換部４０に印加されアナログ信号に変換される。従って、ディジタルーアナログ変換部４０の出力信号は明るさと対比が訂正された映像信号となる。図５の回路はｎＡＰＬ値が計算されたフレームと実際にルックアップテーブル部３０に入力されたフレームが相違になるが、一般に隣接フレーム間の映像信号は緩やかに変わるので問題とならない。しかし、場面転換のような急激な映像信号の変化が生じたり、ｎＡＰＬが求められた映像信号について明るさ訂正を願う場合、遅延素子をアナログーディジタル変換部１０とルックアップテーブル部３０との間に連結すれば良い。かかる遅延素子はｎＡＰＬが計算される期間の間アナログーディジタル変換部１０から出力される映像信号を遅延させる。

【００２２】図６は本発明の場面適応映像改善回路の第２実施例を示したブロック構成図である。図６の映像改善回路は図５のブロックと同一な構成及び機能を有するブロックについて図５と同一な部材番号を付した。ただし、アナログーディジタル変換部１０とルックアップテーブル部３０との間に増幅部５０が新たに追加された。この増幅部５０はＡＰＬ計算部２０から出力されたｎＡＰＬ値により決定される可変的な増幅率でアナログーディジタル変換部１０から出力された映像信号を増幅してルックアップテーブル部３０に出力する。

【００２３】図７は前記増幅部５０の入出力特性曲線を示したグラフである。増幅部５０はＡＰＬ計算部２０から印加されたｎＡＰＬ値が１に近くの値の場合はｓ３方向に入力映像信号の増幅を変化させ、その反対の場合はｓ２方向に変化させる。これは極端の明るさを有する画面状態の入力映像信号のレベルを調整することにより図５の装置に比べて補正効率を高めるためである。

【００２４】図８は本発明の場面適応映像改善回路の第３実施例を示したブロック構成図である。図８の映像改善回路は図５のブロックと同一な構成及び機能を有するブロックについて図５と同一な部材番号を付した。しかし、図５のＡＰＬ計算部２０は低域通過フィルタ６０及びディコーダ７０に代替された。低域通過フィルタ６０は時定数が相当大きいフィルタでなされた場合近似したｎＡＰＬ値を求められ、水平同期期間と垂直ブランキン

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グ期間など実際に画像でない部分の値を大略計算して引いた値に補正が可能である。低域通過フィルタ６０は１フレーム期間または多数のフレーム期間の間の実際映像信号区間に対する入力映像信号のｎＡＰＬ値を計算する。計算されたｎＡＰＬ値は電圧の形態でディコーダ７０に出力する。ディコーダ７０は前記低域通過フィルタ６０から印加された電圧によりルックアップテーブル部３０を制御するための信号を出力する。

【００２５】

【発明の効果】以上述べたように、本発明は入力映像信号の平均明るさレベルの値により入出力特性を相異なるようにして明るさを適応的に補正することにより、対比が改善された映像信号が得られ、急激な明るさ変化を制限して極端に暗い画面も自然に表現でき、特定ｎＡＰＬ領域では対比調節のみを行って明るさと対比表現の向上された画像が得られる。また、映像信号の増幅率を調整して明るさと対比の補正効率を向上させうる。

【図面の簡単な説明】

【図１】従来の対比訂正装置に使われた入出力特性を示したグラフである。

【図２】従来の画像明るさ調節回路に使われた明るさ訂

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正特性を示すグラフである。

【図３】本発明に使われた入出力特性を示すグラフである。

【図４】本発明の場面適応映像改善方法における明るさ訂正特性を示すグラフである。

【図５】本発明の場面適応映像改善回路の第１実施例を示すブロック構成図である。

【図６】本発明の場面適応映像改善回路の第２実施例を示すブロック構成図である。

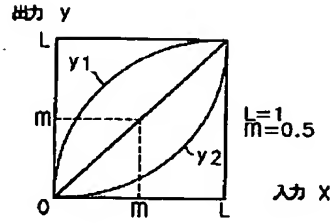
【図７】図６の増幅部による入出力特性曲線を示すグラフである。

【図８】本発明の場面適応映像改善回路の第３実施例を示すブロック図構成図である。

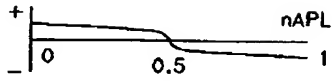
【符号の説明】

１０　アナログーディジタル変換部
２０　ｎＡＰＬ計算部
３０　ルックアップテーブル部
４０　ディジタルーアナログ変換部
５０　増幅部
６０　低域通過フィルタ
７０　ディコーダ

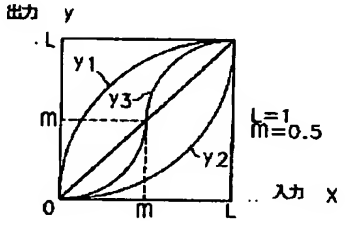
【図１】



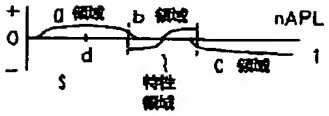
【図２】



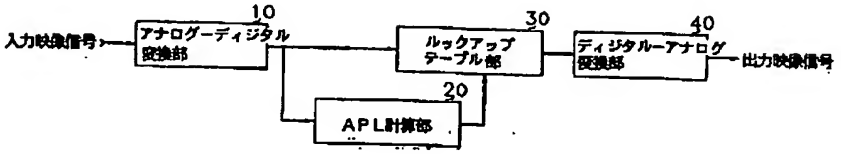
【図３】



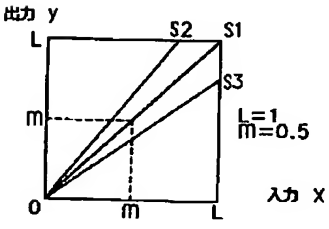
【図４】



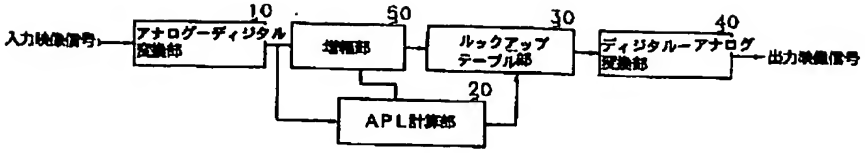
【図５】



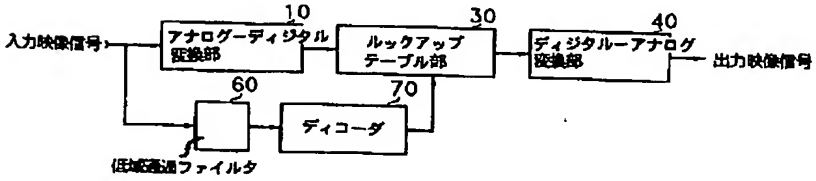
【図７】



【図６】


入力映像信号
10
アナログーディジタル
変換部
50
増幅部
30
ルックアップ
テーブル部
40
ディジタルーアナログ
変換部
出力映像信号
20
APL計算部

【図８】


入力映像信号
10
アナログーディジタル
変換部
30
ルックアップ
テーブル部
40
ディジタルーアナログ
変換部
出力映像信号
60
70
ディコーダ
低域変通ファイルタ

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] A gradation compensator characterized by providing the following A histogram memory which memorizes a histogram of an image luminance signal A histogram arithmetic circuit which considers an output signal of this histogram memory as an input, and extracts the feature of a histogram from this data A limiter and an adder circuit which is connected to an outgoing end of this histogram arithmetic circuit, and processes data of the above-mentioned histogram memory An accumulation control register circuit and a normalization control register circuit which were connected to an outgoing end of the above-mentioned histogram arithmetic circuit, respectively, A histogram accumulation circuit which inputs an output signal of the above-mentioned histogram memory, and an output signal of an accumulation control register circuit, and carries out accumulation of the processed data of the above-mentioned histogram memory, An accumulation histogram memory which memorizes a result which carried out accumulation, and a look-up table arithmetic circuit which inputs an output signal of this accumulation histogram memory, and an output signal of a normalization control register circuit, and normalizes data of an accumulation histogram memory, Look-up table memory which memorizes this result of an operation, and a buffer in which it connects with an outgoing end of the above-mentioned histogram memory, and histogram data in front of 1 vertical-scanning period is stored, The constant twice circuit connected to an outgoing end of this buffer, an adder which adds output data of the above-mentioned histogram memory, and output data of a constant twice circuit, and inputs this addition result into a histogram memory, and a timing-control circuit which controls each above-mentioned circuit
[Claim 2] A gradation compensator characterized by providing the following A histogram memory which memorizes a histogram of an image luminance signal A histogram arithmetic circuit which considers an output signal of this histogram memory as an input, and extracts the feature of a histogram from this data A limiter and an adder circuit which is connected to an outgoing end of this histogram arithmetic circuit, and processes data of the above-mentioned histogram memory An accumulation control register circuit and a normalization control register circuit which were connected to an outgoing end of the above-mentioned histogram arithmetic circuit, respectively, A histogram accumulation circuit which inputs an output signal of the above-mentioned histogram memory, and an output signal of an accumulation control register circuit, and carries out accumulation of the processed data of the above-mentioned histogram memory, An accumulation histogram memory which memorizes a result which carried out accumulation, and a look-up table arithmetic circuit which considers an output signal of this accumulation histogram memory, and an output signal of a normalization control register circuit as an input, and normalizes data of an accumulation histogram memory, Look-up table memory which memorizes this result of an operation, and a buffer in which it connects with an outgoing end of the above-mentioned histogram memory, and histogram data in front of 1 vertical-scanning period is stored, A circuit which is connected to an outgoing end of the above-mentioned histogram memory, and detects change of an image scene, The constant twice circuit where an output signal of the above-mentioned buffer is considered as an input, and a value of a coefficient changes with the output signals of the above-mentioned image scene change detector, An adder which adds output data of the above-

mentioned histogram memory, and output data of a constant twice circuit, and inputs this addition result into a histogram memory, and a timing-control circuit

[Claim 3] A gradation compensator characterized by providing the following A histogram memory which memorizes a histogram of an image luminance signal A histogram arithmetic circuit which considers an output signal of this histogram memory as an input, and extracts the feature of a histogram from this data A limiter and an adder circuit which is connected to an outgoing end of this histogram arithmetic circuit, and processes data of the above-mentioned histogram memory An accumulation control register circuit and a normalization control register circuit which were connected to an outgoing end of the above-mentioned histogram arithmetic circuit, respectively, A histogram accumulation circuit which considers an output signal of the above-mentioned histogram memory, and an output signal of an accumulation control register circuit as an input, and carries out accumulation of the processed data of the above-mentioned histogram memory, An accumulation histogram memory which memorizes a result which carried out accumulation, and a look-up table arithmetic circuit which considers an output signal of this accumulation histogram memory, and an output signal of a normalization control register circuit as an input, and normalizes data of an accumulation histogram memory, An adder adding output data of this look-up table arithmetic circuit, and output data of the following constant twice circuit, Look-up table memory which memorizes output data of this adder, a buffer in which data in front of 1 vertical-scanning period of this look-up table memory is stored, said constant twice circuit which is connected to an outgoing end of this buffer and outputs the result of an operation to the above-mentioned adder, and a timing-control circuit

[Claim 4] A gradation compensator characterized by providing the following A histogram memory which memorizes a histogram of an image luminance signal A histogram arithmetic circuit which considers an output signal of this histogram memory as an input, and extracts the feature of a histogram from this data A limiter and an adder circuit which is connected to an outgoing end of this histogram arithmetic circuit, and processes data of the above-mentioned histogram memory An accumulation control register circuit and a normalization control register circuit which were connected to an outgoing end of the above-mentioned histogram arithmetic circuit, respectively, A histogram accumulation circuit which considers a signal as an input and carries out accumulation of the processed data of the above-mentioned histogram memory to an output signal of the above-mentioned histogram memory, and an output of an accumulation histogram register circuit, An accumulation histogram memory which memorizes a result which carried out accumulation, and a look-up table arithmetic circuit which considers an output signal of this accumulation histogram memory, and an output signal of a normalization control register circuit as an input, and normalizes data of an accumulation histogram memory, An adder adding output data of this look-up table arithmetic circuit, and output data of a constant twice circuit, Look-up table memory which memorizes output data of this adder, A buffer in which data in front of 1 vertical-scanning period of this look-up table is stored, The above-mentioned constant twice circuit which is connected to an outgoing end of this buffer and outputs the result of an operation to the above-mentioned adder, a circuit which detects change of an image scene which is connected to an outgoing end of the above-mentioned look-up table arithmetic circuit, and controls said coefficient of a constant twice circuit, and a timing-control circuit

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[Translation done.]

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the gradation compensator used when amending the gradation of a video signal of a television receiver, a video tape recorder, etc.
[0002]
[Description of the Prior Art] In recent years, by letting a video signal pass to nonlinear amplifier, in order to show an image more vividly with enlargement of a color-television receiving set, and high-definition-izing, a gradation compensator amends the gradation of a video signal, and importance has been attached to it in order to expand the dynamic range of the image on CRT.
[0003] Below, the conventional gradation compensator is explained. Drawing 5 shows the block diagram of the conventional gradation compensator. In drawing 5 , 1 is an A-D converter which changes an input luminance signal into digital value. 2 is a histogram memory which takes the luminance distribution of an input luminance signal, and an intensity level is made for frequency to go into the data to the address of memory generally. 3 is a histogram arithmetic circuit, it computes average [of an input luminance signal], mode value, minimum value, maximum, deflection coefficient, sober product, and black area etc. from the data of a histogram memory 2, calculates each control value, such as limiter level, an aggregate value, an accumulation start intensity level, an accumulation stop intensity level, and the maximum intensity level, by the result, and outputs it to a limiter and an adder circuit 5, the accumulation control register circuit 6, and the normalization control register circuit 7. A limit is added or above-mentioned limiter and adder circuit 5 perform an add operation so that it may not become with the data transmitted from the histogram arithmetic circuit 3 more than level with the data of a histogram. Data processing is finished while the address is generally accessed once. In case the above-mentioned accumulation control register circuit 6 asks for an accumulation histogram, the intensity level which begins the accumulation, and the intensity level which stops accumulation are given to it from the histogram arithmetic circuit 3, and it controls the histogram accumulation circuit 8. The above-mentioned histogram accumulation circuit 8 accumulates the processed data of a histogram memory 2 with the control signal of the accumulation control register circuit 6. 9 is an accumulation histogram memory and memorizes the accumulation result of the histogram accumulation circuit 8. An intensity level is made for frequency to go into the data to the address of memory generally. In case the above-mentioned normalization control register circuit 7 normalizes the data of an accumulation histogram and creates a look-up table, the maximum intensity level of the output luminance signal after the normalization is given to it from the histogram arithmetic circuit 3, and it controls a normalization coefficient according to the value. 10 is a look-up table arithmetic circuit, and normalizes the data of the accumulation histogram memory 9 based on the output signal of the normalization control register circuit 7. 11 is look-up table memory and memorizes the data normalized in the look-up table arithmetic circuit 10. An input intensity level is gone into the address of memory, and an amendment output intensity level is made to go into the data generally. 12 is a timing-control circuit and performs sequence of each operation, control of each memory, etc. 13 is a DA converter and changes into an analog value

the output luminance signal of the digital value amended by the look-up table.
[0004] About the gradation amendment circuit constituted as mentioned above, the actuation is explained below. The wave of each part of operation is illustrated to drawing 6 .
[0005] First, the input luminance signal a is inputted into A-D converter 1, and it changes into digital value, and outputs as a conversion input luminance signal b. A histogram memory 2 makes the address this conversion input luminance signal b, and processes data in a limiter and an adder circuit 5. Histogram distribution of the input luminance signal a can be taken by performing this actuation during the 1 vertical scanning. This is shown in drawing 6 (a).
[0006] Next, the histogram arithmetic circuit 3 reads the data of a histogram memory 2 containing this histogram distribution, and average [of an input luminance signal], mode value, minimum value, maximum, deflection coefficient, sober product, and black area etc. is calculated. And each control value, such as limiter level, an aggregate value, a start intensity level of accumulation count and a stop intensity level, and the maximum intensity level after normalization, is calculated from these count results, and these data is transmitted to a limiter and an adder circuit 5, the accumulation control register circuit 6, and the normalization control register circuit 7.
[0007] Next, a limiter and an adder circuit 5 read data from a histogram memory 2, calculates a limiter (drawing 6 (b)), addition, etc. based on each data transmitted from the histogram arithmetic circuit 3 to each data, and outputs the result (amendment histogram data c) to the histogram accumulation circuit 8 (drawing 6 (c)). Here, when an aggregate value is fixed, it becomes close to histogram flattening processing, so that it becomes [an accumulation curve] close to a straight line and is so small that the value is large (drawing 6 (c), drawing 6 (d)).
[0008] And with the accumulation start intensity level and accumulation stop intensity level which are given from the accumulation control register circuit 6, the histogram accumulation circuit 8 calculates the accumulation histogram data f of the amendment histogram data c about within the limits of it, and memorizes this result to the accumulation histogram memory 9.
[0009] Next, the look-up table arithmetic circuit 10 reads data from the accumulation histogram memory 9, it asks for a normalization coefficient so that it may be set to maximum output intensity-level h to which the maximum of that accumulation histogram data g is given from the normalization control register circuit 7, it calculates to all the accumulation histogram data g by this coefficient, and, as a result, memorizes i in the look-up table memory 11. At this time, actuation like automatic contrast control (ACL) and automatic bright control (ABL) can be performed by controlling maximum output intensity-level h. This actuation is shown in drawing 6 (e).
[0010] Next, the look-up table memory 11 reads that data by making the conversion input luminance signal b into the address, and outputs this data as an amendment output luminance signal j (drawing 6 (f) is the histogram of the amendment output luminance signal j.). And DA converter 13 changes and outputs this amendment output luminance signal j to analog signal k.
[0011] The timing-control circuit 12 controls actuation of each circuit so that actuation of each part is performed to timing which was described above. (For example, refer to Japanese Patent Application No. No. 265393 [one to] concerning application of the same applicant "a gradation compensator")
[0012]
[Problem(s) to be Solved by the Invention] However, with the above-mentioned conventional configuration, since each control signal computed in a histogram arithmetic circuit was the instantaneous value computed from histogram distribution of 1 vertical-scanning period, it had the trouble that the output luminance signal which these values were changed sharply, consequently was amended by the noise included in a video signal vibrated.
[0013] This invention does not solve the above-mentioned conventional trouble, and while offering the gradation compensator which performs smooth amendment to which an amendment output luminance signal does not vibrate, it follows in footsteps of change of an image scene, and it aims at offering a gradation compensator which is not in an output response.
[0014]
[Means for Solving the Problem] In order to attain this purpose a gradation compensator of this

invention A histogram memory and a histogram arithmetic circuit connected to an outgoing end of this histogram memory, A limiter, an adder circuit, an accumulation control register circuit, and a normalization control register circuit which were connected to an outgoing end of this histogram arithmetic circuit, respectively, A histogram accumulation circuit where an outgoing end of the above-mentioned histogram memory and an outgoing end of an accumulation control register circuit were connected, An accumulation histogram memory connected to an outgoing end of this histogram accumulation circuit, A look-up table arithmetic circuit where an outgoing end of this accumulation histogram memory and an outgoing end of a normalization control register circuit were connected, Look-up table memory which memorizes this result of an operation, and a buffer connected to an outgoing end of the above-mentioned histogram memory, The constant twice circuit connected to an outgoing end of this buffer, an output signal of the above-mentioned histogram memory, and an output signal of a constant twice circuit are inputted, and it consists of an adder by which an outgoing end was connected to an input edge of a histogram memory, and a timing-control circuit.

[0015] Moreover, a histogram arithmetic circuit where a gradation compensator of this invention was connected to an outgoing end of a histogram memory and this histogram memory, A limiter, an adder circuit, an accumulation control register circuit, and a normalization control register circuit which were connected to an outgoing end of this histogram arithmetic circuit, respectively, A histogram accumulation circuit where an outgoing end of the above-mentioned histogram memory and an outgoing end of an accumulation control register circuit were connected, An accumulation histogram memory connected to an outgoing end of this histogram accumulation circuit, A look-up table arithmetic circuit where an outgoing end of this accumulation histogram memory and an outgoing end of a normalization control register circuit were connected, Look-up table memory which memorizes the result of an operation not coming, and a buffer connected to an outgoing end of the above-mentioned histogram memory, respectively and an image scene change detector, The constant twice circuit where an outgoing end of the above-mentioned buffer was connected to an input edge, and an outgoing end of an image scene change detector was connected to a coefficient control edge, An output signal of the above-mentioned histogram memory and an output signal of a constant twice circuit are inputted, and an outgoing end consists of an adder connected to an input edge of a histogram memory, and a timing-control circuit.

[0016] Moreover, a histogram arithmetic circuit where a gradation compensator of this invention was connected to an outgoing end of a histogram memory and this histogram memory, A limiter, an adder circuit, an accumulation control register circuit, and a normalization control register circuit which were connected to an outgoing end of this histogram arithmetic circuit, respectively, A histogram accumulation circuit where an outgoing end of the above-mentioned histogram memory and an outgoing end of an accumulation control register circuit were connected, An accumulation histogram memory connected to an outgoing end of this histogram accumulation circuit, A look-up table arithmetic circuit where an outgoing end of this accumulation histogram memory and an outgoing end of a normalization control register circuit were connected, An adder which considers an output signal of this look-up table arithmetic circuit, and an output signal of a constant twice circuit as an input, It consists of look-up table memory connected to an outgoing end of this adder, a buffer in which an output of this look-up table memory is stored, a constant twice circuit connected to an outgoing end of this buffer, and an input edge of the above-mentioned adder, and a timing-control circuit.

[0017] Moreover, a histogram arithmetic circuit where a gradation compensator of this invention was connected to an outgoing end of a histogram memory and this histogram memory, A limiter, an adder circuit, an accumulation control register circuit, and a normalization control register circuit which were connected to an outgoing end of this histogram arithmetic circuit, respectively, A histogram accumulation circuit where an outgoing end of the above-mentioned histogram memory and an outgoing end of an accumulation control register circuit were connected, An accumulation histogram memory connected to an outgoing end of this histogram accumulation circuit, A look-up table arithmetic circuit where an outgoing end of this accumulation histogram memory and an outgoing end of a normalization control register circuit were connected, An adder which takes the sum of an output signal of this look-up

table arithmetic circuit, and an output signal of a constant twice circuit, Look-up table memory which considers an output signal of this adder as an input, A buffer in which an output of this look-up table memory is stored, and the constant twice circuit connected to an outgoing end of this buffer, and an input edge of an adder, It consists of an image scene change detector where it connected with an outgoing end of the above-mentioned look-up table arithmetic circuit, and the outgoing end was connected to a coefficient control edge of a constant twice circuit, and a timing-control circuit.

[0018]

[Function] By these configurations, by letting the data of histogram distribution used in order to create a look-up table pass in a recursive filter circuit, fluctuation of each control signal by the noise which the time constant of change of histogram distribution becomes large, and is included in the video signal inputted can be suppressed, consequently vibration of an amendment output luminance signal can be stopped.

[0019] Moreover, even if each control signal is incorrect-detected and a look-up table vibrates greatly by a noise etc. by letting the data of a look-up table pass in a recursive filter circuit, smooth amendment can be performed with a feedback staff's time constant, without an amendment output luminance signal vibrating.

[0020] Furthermore, by detecting change of an image scene and changing the coefficient of the constant twice circuit which constitutes a recursive filter circuit according to the rate of the change, when for example, an image scene changes rapidly, the delay of an output response can be abolished by setting the coefficient to 0.

[0021]

[Example] (Example 1) One example of this invention is explained hereafter, referring to a drawing.

[0022] In drawing 1 , a histogram memory and 3 are histogram arithmetic circuits, and an A-D converter and 2 of 1 are the same as that of the conventional example. 21 is a buffer and stores the histogram data extracted before 1 vertical-scanning period. 22 is a constant twice circuit and carries out the multiplication of the constant in the input signal supplied from a buffer 21. 23 is an adder and performs addition with the output signal of the constant twice circuit 22, and the output signal of a histogram memory 2. The addition output signal is inputted into the histogram memory 2. Other circuitry is the same as that of drawing 5 .

[0023] The actuation is explained about the gradation compensator constituted as mentioned above. First, before beginning 1 vertical-scanning period sample newly, the data already memorized by the histogram memory 2 is transmitted to a buffer 21, and the interior of a histogram memory 2 is cleared. Then, it newly samples. After the sampling of 1 vertical-scanning period is completed, the data of a histogram memory 2 is read one by one. And the data of the output-data r and the intensity level corresponding to this is read from a buffer 21, and the data s which carried out the multiplication of the coefficient which is the constant twice circuit 22 is added with an adder 23. The addition result t is written in a histogram memory 2, and histogram distribution is updated. Henceforth, each control signal is computed based on this updated histogram distribution in the histogram arithmetic circuit 3, it asks for an accumulation histogram, and a look-up table is created.

[0024] According to this example, fluctuation of the histogram distribution by the noise included in an input signal can be controlled a buffer 21, the constant twice circuit 22, and by forming an adder 23 as mentioned above.

[0025] (Example 2) Next, it explains, referring to a drawing about the 2nd example of this invention.

[0026] In drawing 2 , as for a buffer and 22, a constant twice circuit and 23 are adders, and a histogram memory and 21 of 2 are the same as that of the configuration of drawing 1 . Differing from the configuration of drawing 1 is the point of having formed the image scene change detector 24, having connected the input edge to the outgoing end of a histogram memory 2, and having connected the outgoing end of the image scene change detector 24 to the coefficient control edge of the constant twice circuit 22.

[0027] The actuation is explained about the gradation compensator constituted as mentioned above. Fundamental actuation is the same as that of an example 1. Differing from an example 1 compares the

minimum value of the present histogram first memorized by the minimum value and the histogram memory 2 of a histogram before accumulating in a buffer 21 in the image scene change detector 24, and it changes the coefficient of the constant twice circuit 22 according to the magnitude of the difference. For example, when the difference is large (i.e., when an image scene changes suddenly), a coefficient is set to 0, and it calculates based on the momentary histogram distribution memorized by the histogram memory 2.

[0028] According to this configuration, it can amend a buffer 21, the constant twice circuit 22, an adder 23, and by forming the image scene change detector 24, without the response of the final output being overdue by changing the coefficient of a feedback system, when an image scene changes suddenly.

[0029] In addition, in the image scene change detector 24, although detection of change of an image scene was performed from the minimum value of a histogram, it can carry out from maximum, the average, etc.

[0030] (Example 3) Next, it explains, referring to a drawing about the 3rd example of this invention.

[0031] In drawing 3 , 10 is a look-up table arithmetic circuit, 11 is look-up table memory, and it is the same as that of the conventional example. 34 is a buffer and stores the data of the look-up table memory 11 in front of 1 vertical-scanning period. 31 carries out the multiplication of the constant in the input signal supplied from a buffer 34 in a constant twice circuit. 32 is an adder and adds the output signal of the look-up table arithmetic circuit 10, and the output signal of the constant twice circuit 31. He is trying to supply the output signal of the adder to the look-up table memory 11. Other configurations are the same as that of drawing 5 .

[0032] The actuation is explained about the gradation compensator constituted as mentioned above. In case renewal of sequential of the contents of the look-up table memory 11 is carried out, the data of the look-up table memory 11 in front of 1 vertical-scanning period already stored is first transmitted to a buffer 34, and the interior of the look-up table memory 11 is cleared. Next, translation data u computed in the look-up table arithmetic circuit 10 is read one by one, and the data of the intensity level corresponding to this is read from a buffer 34. The multiplication of the constant value which is the constant twice circuit 31 is carried out, and output-data t of a buffer 34 is added with translation data u, and, as a result, writes w in the look-up table memory 11.

[0033] According to this configuration, the constant twice circuit 31 and an adder 32 constitute a recursive filter circuit, and vibration of a look-up table can be controlled with the time constant.

[0034] (Example 4) Next, it explains, referring to a drawing about the 4th example of this invention.

[0035] In drawing 4 , as for a buffer and 31, look-up table memory and 34 are [a constant twice circuit and 32] adders, and a look-up table arithmetic circuit and 11 of 10 are the same as that of the configuration of drawing 3 . Differing from the configuration of drawing 3 is the point of having formed the image scene change detector 33, having connected the input edge to the outgoing end of the look-up table arithmetic circuit 10, and having connected the outgoing end of the image scene change detector 33 to the coefficient control edge of the constant twice circuit 31.

[0036] The actuation is explained about the gradation compensator constituted as mentioned above. Fundamental actuation is the same as that of an example 3. Differing from an example 3 compares with the corresponding maximum of the difference of an intensity level the maximum of the difference which subtracted the intensity level which corresponds first from the look-up table data computed from the histogram in front of 1 vertical-scanning period in the image scene change detector 33, and the look-up table data computed from the current histogram, and it changes the coefficient of the constant twice circuit 31 according to the magnitude of the difference. For example, when the difference is large (i.e., when an image scene changes suddenly), a coefficient is set to 0 and the instantaneous value u of the look-up table computed now is written in the look-up table memory 11.

[0037] According to this configuration, a buffer 34, the constant twice circuit 31, an adder 32, and by forming the image scene change detector 33, the coefficient of the constant twice circuit 31 is made small at the time of sudden change of an image scene, and it can amend, without the response of the final output being overdue by writing momentary detection data in a look-up table.

[0038] In addition, in the image scene change detector 33, although detection of change of an image

scene was performed from the maximum of the difference of the data of a look-up table, it can also carry out from the inclination of a conversion curve, a turnoff point, etc.

[0039]

[Effect of the Invention] The histogram arithmetic circuit where this invention was connected to the outgoing end of a histogram memory and this histogram memory as mentioned above, The limiter, the adder circuit, accumulation control register circuit, and normalization control register circuit which were connected to the outgoing end of this histogram arithmetic circuit, respectively, The outgoing end of the above-mentioned histogram memory, and the histogram accumulation circuit where outgoing end drawing connection of the accumulation control register circuit was made, The accumulation histogram memory connected to the outgoing end of this histogram accumulation circuit, The look-up table arithmetic circuit where the outgoing end of this accumulation histogram memory and the outgoing end of a normalization control register circuit were connected, The look-up table memory which memorizes this result of an operation, and the buffer connected to the outgoing end of the above-mentioned histogram memory, By adding the constant twice circuit connected to the outgoing end of this buffer, output signal of the above-mentioned histogram memory, and the output signal of a constant twice circuit, and preparing the adder which supplies that addition result to a histogram memory, and a timing-control circuit Fluctuation of the histogram distribution by the noise included in a video signal can be controlled, and the outstanding gradation compensator with which the amended output signal does not vibrate can be realized.

[0040] Furthermore, a histogram memory and the histogram arithmetic circuit connected to the outgoing end of this histogram memory, The limiter, the adder circuit, accumulation control register circuit, and normalization control register circuit which were connected to the outgoing end of this histogram arithmetic circuit, respectively, The histogram accumulation circuit where the outgoing end of an accumulation control register circuit was connected to the outgoing end of the above-mentioned histogram memory, The accumulation histogram memory connected to the outgoing end of this histogram accumulation circuit, The look-up table arithmetic circuit where the outgoing end of this accumulation histogram memory and the outgoing end of a normalization control register circuit were connected, The look-up table memory which memorizes this result of an operation, and the buffer connected to the outgoing end of the above-mentioned histogram memory, respectively and an image scene change detector, The constant twice circuit where the output value of the above-mentioned buffer was connected to the input value, and the outgoing end of an image scene change detector was connected to the coefficient control edge, By adding the output signal of the above-mentioned histogram memory, and the output signal of a constant twice circuit, and preparing the adder which supplies the addition output as an input of a histogram memory, and a timing-control circuit According to change of an image scene, the delay of an output response can be abolished by changing the coefficient of a feedback system, and the outstanding gradation compensator which can perform gradation amendment which followed in footsteps of change of an image scene can be realized.

[0041] Moreover, a histogram memory and the histogram arithmetic circuit connected to the outgoing end of this histogram memory, The limiter, the adder circuit, accumulation control register circuit, and normalization control register circuit which were connected to the outgoing end of this histogram arithmetic circuit, respectively, The histogram accumulation circuit where the outgoing end of the above-mentioned histogram memory and the outgoing end of an accumulation control register circuit were connected, The accumulation histogram memory connected to the outgoing end of this histogram accumulation circuit, The look-up table arithmetic circuit where the outgoing end of this accumulation histogram memory and the outgoing end of a normalization control register circuit were connected, The adder adding the output signal of this look-up table arithmetic circuit, and the output signal of a constant twice circuit, The look-up table memory connected to the outgoing end of this adder, and the buffer connected to the outgoing end of this look-up table memory, By preparing the constant twice circuit connected between the outgoing end of this buffer, and the input edge of an adder, and a timing-control circuit The fluctuation of the last look-up table which the look-up table by incorrect detection of each control signal flusters, and is written in memory as **** can be controlled, and the outstanding

gradation compensator which performs smooth gradation amendment can be realized.
[0042] Furthermore, a histogram memory and the histogram arithmetic circuit connected to the outgoing end of this histogram memory, The limiter, the adder circuit, accumulation control register circuit, and normalization control register circuit which were connected to the outgoing end of this histogram arithmetic circuit, respectively, The histogram accumulation circuit where the outgoing end of the above-mentioned histogram memory and the outgoing end of an accumulation control register circuit were connected, The accumulation histogram memory connected to the outgoing end of this histogram accumulation circuit, The look-up table arithmetic circuit where the outgoing end of this accumulation histogram memory and the outgoing end of a normalization control register circuit were connected, The adder adding the output signal of this look-up table arithmetic circuit, and the output signal of a constant twice circuit, The look-up table memory connected to the outgoing end of this adder, and the buffer connected to the outgoing end of this look-up table memory, By preparing the constant twice circuit where the outgoing end of this buffer was connected between the input edges of an adder, and the image scene change detector connected between the outgoing end of the above-mentioned look-up table arithmetic circuit, and the coefficient control edge of a constant twice circuit According to change of an image scene, the outstanding gradation compensator which can perform high-speed gradation amendment which is not in an output response is realizable by changing the coefficient of a recursive filter circuit.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The block diagram of the gradation compensator in the 1st example of this invention
[Drawing 2] The block diagram of the gradation compensator in the 2nd example of this invention
[Drawing 3] The block diagram of the gradation compensator in the 3rd example of this invention
[Drawing 4] The block diagram of the gradation compensator in the 4th example of this invention
[Drawing 5] The block diagram of the conventional gradation compensator
[Drawing 6] The wave form chart explaining actuation of the conventional gradation compensator
[Description of Notations]
21 34 Buffer
22 Constant Twice Circuit
23 Adder
24 Image Scene Change Detector
31 Constant Twice Circuit
32 Adder
33 Image Scene Change Detector

[Translation done.]

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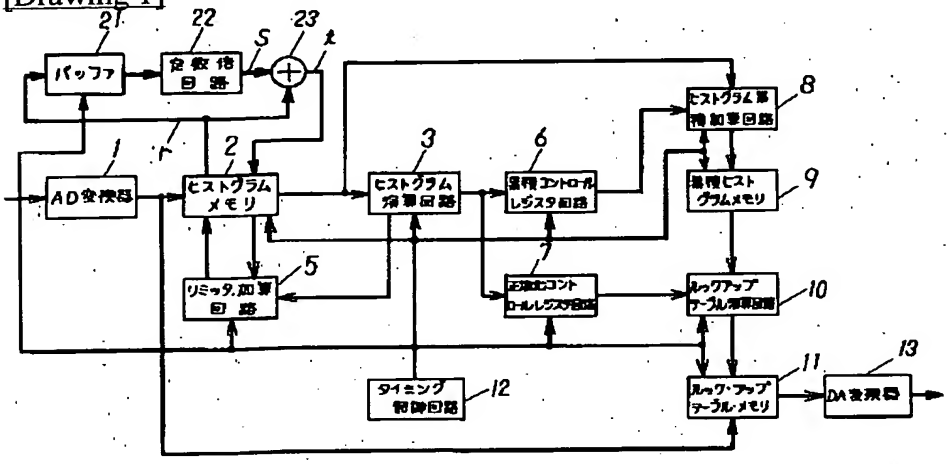
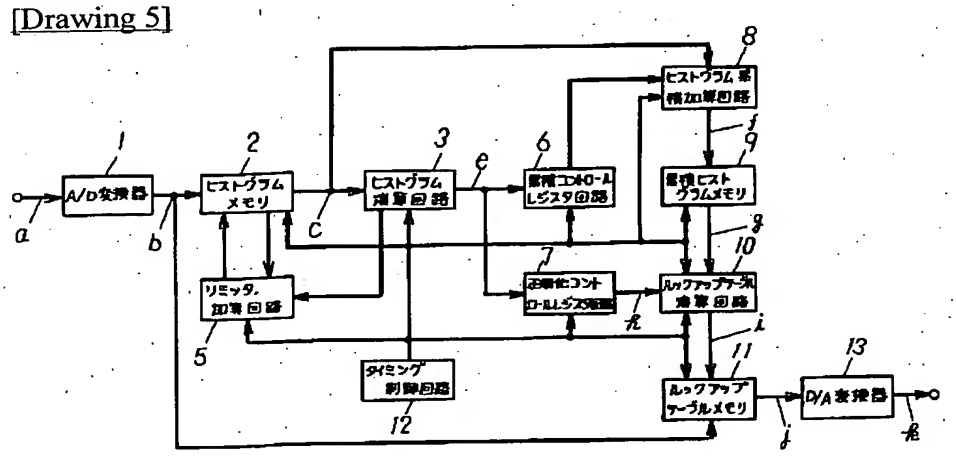
DRAWINGS

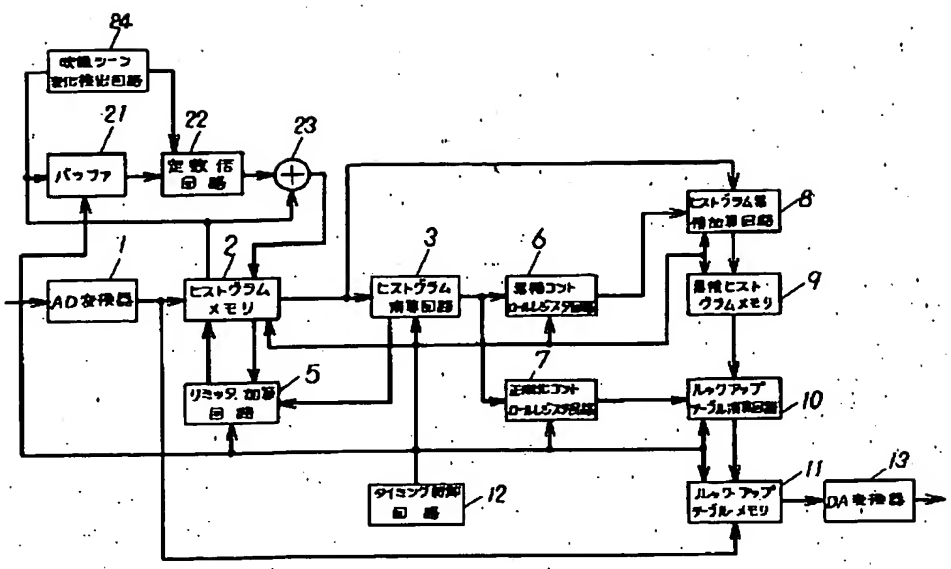
[Drawing 1]



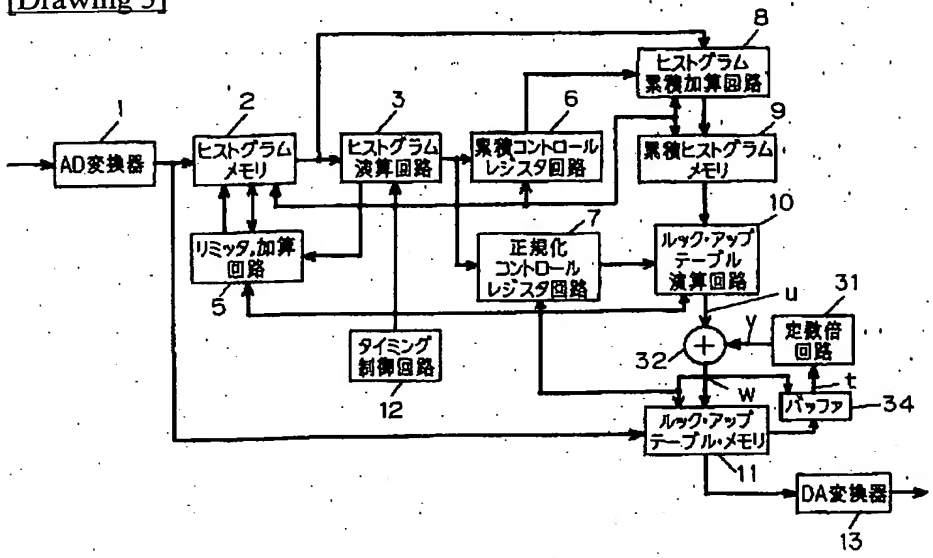
[Drawing 5]



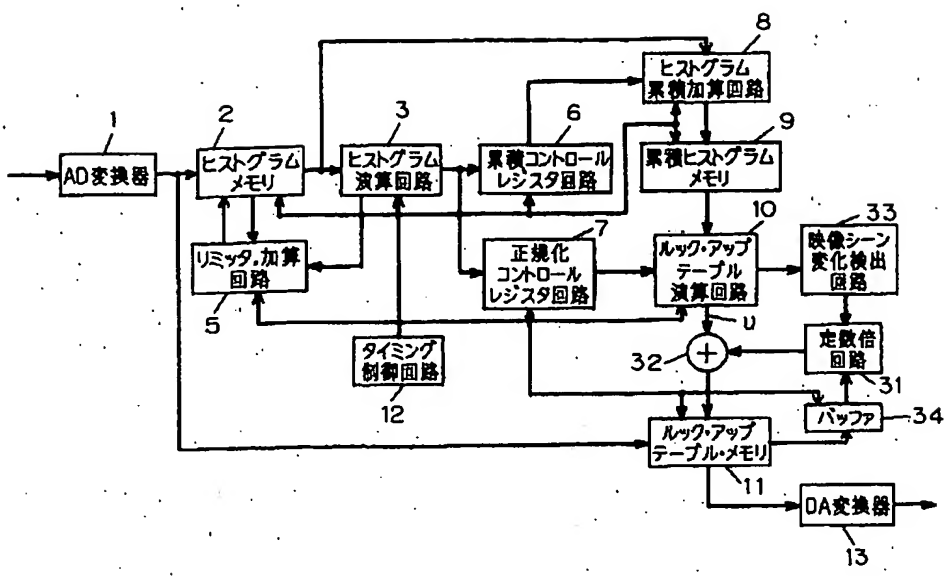
[Drawing 2]



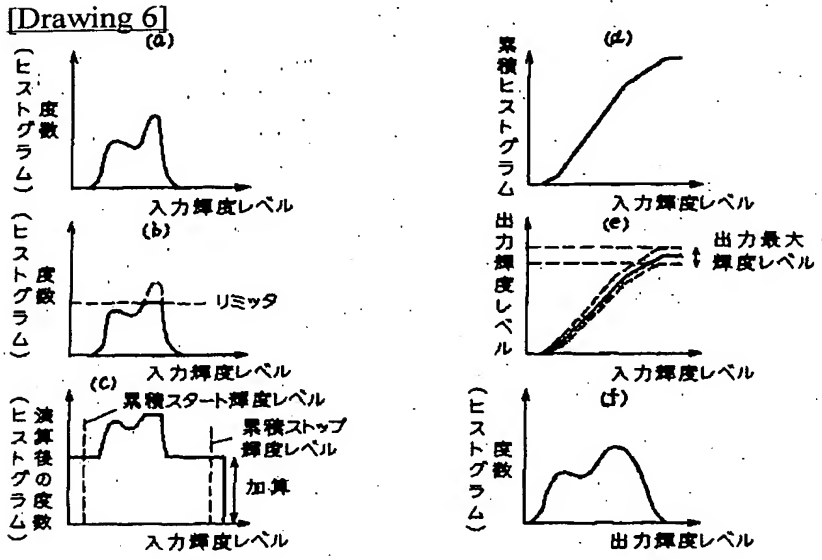
[Drawing 3]



[Drawing 4]



[Drawing 6]



[Translation done.]